REMARKS

Claim 6 is rewritten in independent form with all the limitations of the original claim 1 and original claim 6.

The Examiner objected to the title of the invention.

The Examiner rejected claims 1-6, 8-14 and 16-20 under 35 U.S.C. §102(b) as allegedly being clearly anticipated by Schorn (US Patent No. 6,278,334).

The Examiner rejected claims 7 and 15 under 35 U.S.C. §103(a) as allegedly being unpatentable over Schorn in view of Abe *et al.*

Applicants respectfully traverse the §102 and §103 rejections with the following arguments.

35 U.S.C. §102(b)

The Examiner rejected claims 1-6, 8-14 and 16-20 under 35 U.S.C. §102(b) as allegedly being clearly anticipated by Schorn (US Patent No. 6,278,334).

Applicants respectfully contend that Schorn does not anticipate claim 1, because Schorn does not teach each and every feature of claim 1. For example, Schorn does not teach "the second resistance adjusting circuit comprises an **n-channel transistor**" of claim 1 (bold emphasis added). More specifically, Schorn only teaches that the second resistance adjusting circuit (upper transistor of 48 in FIG. 4) is a p-channel transistor. In contrast, in claim 1, the second resistance adjusting circuit comprises an n-channel transistor. Based on the preceding arguments, Applicants respectfully maintain that Schorn does not anticipate claim 1, and that claim 1 is in condition for allowance.

Since claim 2 depends from claim 1, which is not anticipated by Schorn as argued above, Applicants contend that claim 2 is likewise in condition for allowance.

Moreover, Schorn does not teach "the first resistance adjusting circuit electrically couples the first switch circuit to the output node" of claim 2. More specifically, Schorn, in FIG. 4, teaches that the first switch circuit (the upper transistor of circuit 46) electrically couples the first resistance adjusting circuit (the lower transistor of circuit 46) to the output node OUT. In contrast, in claim 2, the first resistance adjusting circuit electrically couples the first switch circuit to the output node. Based on the preceding arguments, Applicants respectfully maintain that Schorn does not anticipate claim 2.

In addition, Schorn does not teach "the second resistance adjusting circuit electrically couples the second switch circuit to the output node" of claim 2. More specifically, Schorn, in FIG. 4, teaches that the second switch circuit (the lower transistor of circuit 48) electrically couples

the second resistance adjusting circuit (the upper transistor of circuit 48) to the output node OUT. In contrast, in claim 2, the second resistance adjusting circuit electrically couples the second switch circuit to the output node. Based on the preceding arguments, Applicants respectfully maintain that Schorn does not anticipate claim 2, and that claim 2 is in condition for allowance.

Since claims 3-5 depend from claim 1, which is not anticipated by Schorn as argued above, Applicants contend that claims 3-5 are likewise in condition for allowance.

Claim 6 is rewritten in independent form with all the limitations of the original claim 1 and original claim 6. Schorn does not teach the feature "the inverting circuit comprises a **CMOS inverter**" of claim 6 (bold emphasis added). More specifically, Schorn, from FIG. 2 to FIG. 4, only teaches that the oscillator delay stage circuit comprises the inverting circuit 16 (FIG. 2) or the inverting circuit 44 (FIG. 4) without saying further detail about these inverting circuits 16 and 44. In particular, Schorn does not teach the inverting circuit comprises a **CMOS inverter** as claimed in claim 6 (bold emphasis added). Based on the preceding arguments, Applicants respectfully maintain that Schorn does not anticipate claim 6, and that claim 6 is in condition for allowance.

Since claim 8 depends from claim 1, which is not anticipated by Schorn as argued above, Applicants contend that claim 8 is likewise in condition for allowance.

The Examiner rejected claim 9 under 35 U.S.C. §102(b) as allegedly being clearly anticipated by Schorn (US Patent No. 6,278,334).

Applicants respectfully contend that Schorn does not anticipate claim 9, because Schorn does not teach each and every feature of claim 9. For example, Schorn does not teach "the first resistance adjusting circuit comprises an **n-channel transistor**" of claim 9 (bold emphasis added). More specifically, Schorn only teaches that the first resistance adjusting circuit (upper transistor of 48 in FIG. 4) is a p-channel transistor. In contrast, in claim 9, the first resistance adjusting circuit

comprises an n-channel transistor. Based on the preceding arguments, Applicants respectfully maintain that Schorn does not anticipate claim 9, and that claim 9 is in condition for allowance.

Moreover, Schorn does not teach "the first resistance adjusting circuit electrically couples the first switch circuit to the output node" of claim 9. More specifically, Schorn, in FIG. 4, teaches that the first switch circuit (the lower transistor of circuit 48) electrically couples the first resistance adjusting circuit (the upper transistor of circuit 48) to the output node OUT. In contrast, in claim 9, the first resistance adjusting circuit electrically couples the first switch circuit to the output node. Based on the preceding arguments, Applicants respectfully maintain that Schorn does not anticipate claim 9, and that claim 9 is in condition for allowance.

Since claims 10-12 depend from claim 9, which is not anticipated by Schorn as argued above, Applicants contend that claims 10-12 are likewise in condition for allowance.

Since claim 14 depends from claim 9, which is not anticipated by Schorn as argued above, Applicants contend that claim 14 is likewise in condition for allowance.

Moreover, Schorn does not teach "The oscillator delay stage circuit of claim 1, wherein the inverting circuit comprises a **CMOS inverter**" of claim 14 (bold emphasis added). More specifically, Schorn, from FIG. 2 to FIG. 4, only teaches that the oscillator delay stage circuit comprises the inverting circuit 16 (FIG. 2) or the inverting circuit 44 (FIG. 4) without saying further detail about these inverting circuits 16 and 44. In contrast, in claim 14, the inverting circuit is a CMOS inverter. Based on the preceding arguments, Applicants respectfully maintain that Schorn does not anticipate claim 14, and that claim 14 is in condition for allowance.

The Examiner rejected claim 17 under 35 U.S.C. §102(b) as allegedly being clearly anticipated by Schorn (US Patent No. 6,278,334).

Applicants respectfully contend that Schorn does not anticipate claim 17, because Schorn does not teach each and every feature of claim 17. For example, Schorn does not teach "the resistance adjusting circuit comprises an **n-channel transistor**" of claim 17 (bold emphasis added). More specifically, Schorn, in FIG. 4, only teaches that the resistance adjusting circuit (upper transistor of 48) between the output node (OUT) and the first operating voltage (Vdd) is a p-channel transistor. In contrast, in claim 17, the resistance adjusting circuit between the output node and the first operating voltage comprises an n-channel transistor. Based on the preceding arguments, Applicants respectfully maintain that Schorn does not anticipate claim 17, and that claim 17 is in condition for allowance.

Since claim 18 depends from claim 18, which is not anticipated by Schorn as argued above, Applicants contend that claim 18 is likewise in condition for allowance.

Moreover, Schorn does not teach "the resistance adjusting circuit electrically couples the switch circuit to the output node" of claim 9. More specifically, Schorn, in FIG. 4, teaches that the switch circuit (the lower transistor of circuit 48) electrically couples the resistance adjusting circuit (the upper transistor of circuit 48) to the output node OUT. In contrast, in claim 18, the resistance adjusting circuit electrically couples the switch circuit to the output node. Based on the preceding arguments, Applicants respectfully maintain that Schorn does not anticipate claim 18, and that claim 18 is in condition for allowance.

Since claim 19 depend from claim 17, which is not anticipated by Schorn as argued above, Applicants contend that claim 19 are likewise in condition for allowance.

Since claim 20 depends from claim 17, which is not anticipated by Schorn as argued above, Applicants contend that claim 20 is likewise in condition for allowance.

Moreover, Schorn does not teach "The oscillator delay stage circuit of claim 1, wherein the inverting circuit comprises a **CMOS inverter**" of claim 20 (bold emphasis added). More specifically, Schorn, from FIG.2 to FIG. 4, only teaches that the oscillator delay stage circuit comprises the inverting circuit 16 (FIG. 2) or the inverting circuit 44 (FIG. 4) without saying further detail about these inverting circuits 16 and 44. In contrast, in claim 20, the inverting circuit is a CMOS inverter. Based on the preceding arguments, Applicants respectfully maintain that Schorn does not anticipate claim 20, and that claim 20 is in condition for allowance.

CONCLUSION

Based on the preceding arguments, Applicants respectfully believe that all pending claims and the entire application meet the acceptance criteria for allowance and therefore request favorable action. If the Examiner believes that anything further would be helpful to place the application in better condition for allowance, Applicants invites the Examiner to contact Applicants' representative at the telephone number listed below. The Director is hereby authorized to charge and/or credit Deposit Account 09-0456.

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